REMARKS

Claims 1-8 are pending in this application. By this Amendment, claims 3-4 and 6-7 are amended solely for cosmetic purposes and not to overcome the art of record. No new matter is added.

Applicants appreciate the courtesies extended by the Examiner to the Applicants' representative, Jonathan Kidney, during the Telephonic Interview conducted on August 28, 2002. Applicants respectfully request reconsideration of the application in view of the above amendments and following remarks.

MATTERS OF FORM

The Office Action objects to claims 3-4 and 6-7, asserting informalities. Applicant has amended the claims to obviate the objection. Accordingly, withdrawal of this objection is respectfully requested.

The Office Action rejects claims 1-4 and 6-8 under 35 U.S.C. § 112, first paragraph, asserting that the claims contain subject matter which is not described in the specification in such a way to enable one of ordinary skill in the art to make and/or use the invention. This rejection is respectfully traversed.

Specifically, the Office Action asserts that the language of "delaying is irrespective of the comparison when starting the delay time adjustment" in the rejected claims is not described in the specification. Applicant respectfully directs the Examiner's attention to the Applicant's specification, page 15, lines 29-35, for example, which states the phrase "regardless of a comparison result in the phase comparator 8". Thus, Applicant respectfully submits that this language in the specification corresponds at least in part to

the phrase "irrespective of the comparison" in the claims. As stated in the earlier-filed Response by the Applicant, the MPEP does not require the language of the claims to correspond word-for-word with the language of the specification.

Moreover, Applicant's specification, beginning on page 14, line 15, discusses a prior art difficulty in DLL systems when the clock signal has a higher frequency. Specifically, the dummy circuit 6 may cause a phase of delay clock signal dclk 2B behind the phase of the target clock signal tclk (see page 15, lines 17-19 of the Applicant's specification).

In this event, Applicant's claimed invention enables the lengthening of the delay time in the DLL array 7, regardless of the comparison result in the phase comparator 8, to cause the delay clock signal dclk to lag to match the second triggering level of the target clock signal tclk. See Applicant's specification, page 16, lines 4-23, for example.

Thus, it is respectfully submitted that the language of the rejected claims are supported in the Applicant's specification and one of ordinary skill would understand the operations being claimed. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of this rejection.

The Office Action rejects claims 1-4 and 6-8 under 35 U.S.C. § 112, second paragraph, asserting lack of definiteness. Specifically, the Office Action asserts that the term "an initiation period" is not defined. This rejection is respectfully traversed.

Applicant respectfully directs the Examiner's attention to the actual language recited in the current claims. No recitation of "an initiation period" is recited in the claims. Therefore, Applicant respectfully submits that this rejection is an improper rejection, since there is no basis for this rejection in the claims.

Moreover, the Applicant's specification clearly describes the processes in place

when starting the delay time adjustment. (See discussion above regarding the § 112, first paragraph rejection). Accordingly, for at least the above reasons, Applicant respectfully requests the withdrawal of this rejection.

MERITS

The Office Action rejects claims 1-8 under 35 U.S.C. § 102(e) over Lu (U.S. Patent No. 6,100,735). This rejection is respectfully traversed.

Applicant's independent claim 1 recites a delay time adjusting method of adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other, based on a comparison between phases of the input signal and the output signal, the method comprising the steps of increasing the delay time to adjust the phase of the output signal irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 3 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising the step of adjusting the delay time so that, when a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein

the adjusting of the delay is irrespective of the comparison when starting the step of adjusting of the delay.

Applicant's independent claim 4 recites a delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the method comprising, a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of the input first periodic signal, and a second step of increasing the delay time to adjust the phase of the output second periodic signal so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge in said first step, the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the steps of judging and delaying are irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 5 recites a delay time adjusting circuit for adjusting a delay time of an input signal so that a phase of the input signal and a phase of an output signal match each other between phases based on a comparison of the input signal and said output signal, the circuit comprising, detecting means for detecting a phase difference between the phase of the input signal and the phase of the output signal, and delaying means for increasing a delay time of the phase of the output signal irrespective of the detection of phase difference when starting the delay time

adjustment until the phase difference becomes N periods, where N is an integer other than zero.

Applicant's independent claim 6 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, judging means for judging whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a predetermined rising edge of the input first periodic signal, and delaying means for adjusting the delay time so that, when the phase of the predetermined rising edge of the output second periodic signal is judged to be behind the phase of the predetermined rising edge of the input first periodic signal by the judging means, the predetermined rising edge of the output second periodic signal matches a rising edge of the input first periodic signal, a phase of the rising edge being behind and nearest to the phase of the predetermined rising edge of the output second periodic signal, wherein the steps of judging and delaying are irrespective of the comparison when starting the delay time adjustment.

Applicant's independent claim 7 recites a delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of the input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of the input first periodic signal and the input second periodic signal, the circuit comprising, delaying means for delaying the input first periodic signal so as to generate the output second periodic signal, phase-detecting

means for detecting whether a phase of a predetermined rising edge of the output second periodic signal is behind a phase of a first rising edge of the input first periodic signal; and adjusting means for controlling the delaying means so that, when the phase of the predetermined rising edge is judged to be behind the phase of the first rising edge by the phase-detecting means, the delaying means delays the phase of the output second periodic signal until the phase of the predetermined rising edge and a phase of a second rising edge of the input first periodic signal match each other, the second rising edge being one period behind the first rising edge, wherein the steps of delaying, phase-detecting and adjusting are irrespective of the comparison when starting the delay adjustment.

Lu discloses a delay time adjusting method utilizing a coarse DLL and a fine DLL to generate incremental delay adjustments. As illustrated in Figs. 7A-C of Lu, overadjustment of the phase may occur as a multiple of integral periods. Lu solves this problem by devising a dual-pulse stimulus to the DLL during initialization to prevent double-delay operation. See Fig. 8 and col. 8, lines 37-40, for example. A pair of pulses and a 7-blanking period repeats. The rising edge of the first pulse arms the DLL's phase detector and propagates through the series of delay buffers, allowing phase comparison to occur for the second pulse. The DLL can only phase compare during the second pulse. The DLL is modified so that phase comparison can only occur when the phase detector is armed by the first pulse. The DLL becomes stable at a total delay of 1ICLK period with the bias voltage properly set. See col. 8, lines 46-66, for example. Lu also discloses an arming circuit for the phase detector in the coarse DLL. The arming input prevents phase comparison when low, but allows phase detection when high. See col. 9, lines 12-13 and

19-20, for example.

There is no discussion in Lu concerning ignoring the phase comparison of the first and second periodic signals when starting the delay adjustment. Moreover, Lu's device cannot perform the functions or remedy the deficiencies addressed by the Applicant's claimed invention.

Accordingly, Applicant respectfully submits that Lu does not disclose or suggest all the claimed features of Applicant's invention. Additionally, claims 2 and 8 depend from claims 1 and 7, respectively and are patentable for at least the reasons stated above with respect to claims 1 and 7. Therefore, for at least the above reasons, Applicant respectfully requests the withdrawal of the rejection of claims 1-8 under 35 U.S.C. § 102(e).

CONCLUSION

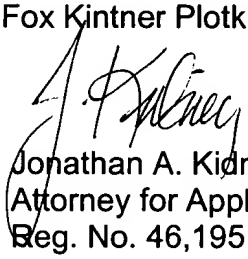
In view of the above remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance is earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge

payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300, referring to client-matter number 100353-00039.

Respectfully submitted,

Arent Fox Kintner Plotkin & Kahn



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Enclosures: Marked-Up Copy of Amended Claims

MARKED-UP COPY OF AMENDED CLAIMS

3. (Thrice Amended) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the method comprising the step of:

adjusting said delay time so that, when a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, wherein the adjusting of said delay is irrespective of said comparison when starting the step of adjusting of said delay.

4. (Thrice Amended) A delay time adjusting method of adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the method comprising:

a first step of judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

a second step of increasing the delay time to adjust said phase of said output second periodic signal so that, when said phase of said predetermined rising edge is

judged to be behind said phase of said first rising edge in said first step, said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the steps of judging and delaying [is] are irrespective of said comparison when starting the delay time adjustment.

6. (Thrice Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

judging means for judging whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a predetermined rising edge of said input first periodic signal; and

delaying means for adjusting said delay time so that, when said phase of said predetermined rising edge of said output second periodic signal is judged to be behind said phase of said predetermined rising edge of said input first periodic signal by said judging means, said predetermined rising edge of said output second periodic signal matches a rising edge of said input first periodic signal, a phase of the rising edge being behind and nearest to said phase of said predetermined rising edge of said output second periodic signal, wherein the steps of judging and delaying [is] are irrespective of said comparison when starting the delay time adjustment.

7. (Thrice Amended) A delay time adjusting circuit for adjusting a delay time of an input first periodic signal so that a phase of said input first periodic signal and a

phase of an output second periodic signal match each other based on a comparison between phases of said input first periodic signal and said input second periodic signal, the circuit comprising:

delaying means for delaying said input first periodic signal so as to generate said output second periodic signal;

phase-detecting means for detecting whether a phase of a predetermined rising edge of said output second periodic signal is behind a phase of a first rising edge of said input first periodic signal; and

adjusting means for controlling said delaying means so that, when said phase of said predetermined rising edge is judged to be behind said phase of said first rising edge by said phase-detecting means, said delaying means delays said phase of said output second periodic signal until said phase of said predetermined rising edge and a phase of a second rising edge of said input first periodic signal match each other, the second rising edge being one period behind said first rising edge, wherein the steps of delaying, phase-detecting and adjusting [is] are irrespective of the comparison when starting the delay adjustment.